Customer No.: 31561
Application No.: 10/707,735
Docket NO.: 11492-US-PA

AMENDMENT

Please amend the application as indicated hereafter.

In the Claims :

1. (original) A flash memory cell, comprising:

a first conductive type substrate;

a second conductive type first well region configured within the first conductive type substrate;

a stacked gate structure disposed over the first conductive type substrate, wherein the stacked gate structure further comprises a tunneling oxide layer, a floating gate, an inter-gate dielectric layer, a control gate and a cap layer sequentially formed over the first conductive type substrate;

a source region and a drain region configured in the first conductive type substrate on each side of the stacked gate structure;

a first conductive type pocket doped region configured within the second conductive type first well region, wherein the first conductive type pocket doped region extends from the drain region to an area underneath the stacked gate structure close to the source region;

a pair of spacers disposed on the sidewalls of the stacked gate structure;

a first conductive type doped region configured within the drain region such that the first conductive type doped region extends through a junction between the drain

region and the first conductive type pocket doped region, wherein the first conductive type doped region separates from the spacer disposed over the drain region by a distance; and

a contact plug disposed over the drain region and connected electrically with the first conductive type doped region.

2. (original) The flash memory cell of claim 1, wherein the first conductive type substrate comprises a p-type substrate.

3. (original) The flash memory cell of claim 1, wherein the second conductive type first well region comprises a deep n-well region.

4. (original) The flash memory cell of claim 1, wherein the first conductive type pocket doped region comprises a p-type pocket doped region.

5. (original) The flash memory cell of claim 1, wherein the first conductive type doped region comprises a p-type doped region.

6. (original) The flash memory cell of claim 1, wherein the source region and the drain region are n-type doped regions.

7. (original) The flash memory cell of claim 1, wherein the drain region and the first conductive type pocket doped region are short-circuit connected.

8. (original) The flash memory cell of claim 1, wherein the distance separating the first conductive type doped region and the spacer is greater than a depth of the drain region.

Claims 9-17 (canceled).